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Gm-boosted Flat Gain UWB Low Noise Amplifier with Noise Cancellation

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This paper presents a high power gain (S_{21}) and low Noise Figure (NF) 3.1-10.6 GHz common gate (CG) CMOS ultra wideband (UWB) low noise amplifier (LNA) using active g_m-boosted technology, T-match input network, self-body-bias, current reused and noise cancelling technique. Wideband input impedance matching was achieved by using the proposed T-match input network to improve the input matching at low frequencies. The proposed UWB LNA employs self-body-bias and current reused technique to decrease the total power consumption. The noise cancelling technique and active gm-boosted technology are utilized to restrain the noise generated and decrease the NF. The proposed LNA was fabricated using TSMC 0.13 μm RF CMOS technology. The simulation results show an average S_{21} of 22.0795 dB with a ripple of ± 0.4125 dB, reverse isolation (S_{12}) was less than -34.15 dB, an excellent NF of 2.232-2.696 dB, input return loss (S_{11}) was less than -15.635 dB and output return loss (S_{22}) was less than -16.903 dB in the frequency range of 3.1-10.6 GHz. The proposed UWB LNA consumed 3.996 mW from a 1.2 V power supply.

1. Introduction

Since the Federal Communication Commission (FCC) has allocated 7.5 GHz bandwidth for UWB application in the unlicensed frequency range of 3.1-10.6 GHz, the related technologies have attracted much attention from both industry and academia, which was confirmed (Lin et al (2007)). This technology has become more popular for broadband wireless communication research due to the main characteristics of UWB systems include low power spectral density, short duration pulses, robustness to multipath fading, and particularly the high data-rate short-range communications.

LNA is the first stage of any communication receiver, so the LNA plays a vital role because the quality of the signal that is received and pre-amplified is a critical factor in the overall system performance, which was confirmed (Wang et al (2007)). The LNA can be directly added to the first stage in the receive path, it usually dominates the NF and bandwidth in the receiver, and it often makes a trade-off among gain, noise and bandwidth, which was confirmed (Wang et al (2011)). Since the emergence of the UWB technology, several CMOS wideband LNA topologies have been presented in LNA designs, such as Zhang and Kinget (2006) and Heydari (2007) reported distributed amplifier, which is usually power hungry and occupy a large area for the use of transmission lines, Reiha (2007) reported resistive shunt feedback, which can achieve good input matching, high gain and wideband performance. Unfortunately, the performance is degraded when the amplifier is operated in the high frequency band, this is due to the effect of parasitic capacitances, which was confirmed (Jung et al (2007) and Chen et al (2008)). Chen (2007) reported cascade amplifiers, and Lin et al (2007) and Muhammed and Rezaul Hasan (2012) reported current reused amplifiers, which is useful for high gain and low power dissipation. However, with the use of a stack of multi-transistors, it increases the required supply voltage, which is not suitable for low supply voltage operation. The UWB LNA has several requirements, such as sufficient wideband input return loss, output return loss, sufficient flat gain over the entire 7.5GHz bandwidth, low noise figure for sensitivity, low power consumption for mobility, and a small chip area for low cost.

In this paper, we present a UWB LNA fabricated in TSMC 0.13 μm RF CMOS technology. The proposed UWB LNA adopts the CG topology and utilizes current reused technique to achieve low power consumption, self-body-bias and current reused technique to decrease the total power consumption, noise cancelling technique

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and active gm-boosted technology to decrease the NF. Rest of this paper is organized as follows. In Section 2, the proposed circuit is analyzed and designed. Simulation methods and results reported in Section 3. Finally, Section 4 presents the conclusion.

2. Circuit analysis and design

2.1 Input impedance matching network

Recently, CG LNAs have become more and more popular for UWB systems thanks to their simpler input matching network (IMN), better linearity, lower power consumption, and better input output isolation compared with CS LNAs, which was confirmed (Liao and Liu (2007)). However, it suffers from channel noise and poor gain response because of the restricted value of the transconductance available for input matching.

Common CG amplifiers set g_m to 20 mS for the input device to achieve broadband input matching. When the g_{m1} value is different from 20 mS, the input impedance cannot match the source impedance. Therefore, we try to alleviate the restricted gm value by a simple IMN topology as shown in Fig.1a. Its equivalent small signal model is shown in Fig. 1b.

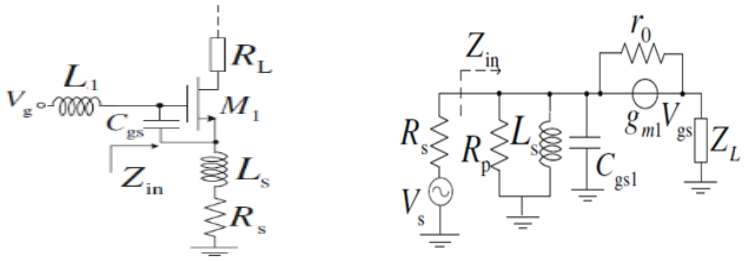
The input impedance looking into the circuit from the source of transistor M_1 is derived as follows:

$$Z_{\text{in}} = jwL_1 + [(j\omega L_S // R_P) // \frac{1}{j\omega C_{gs}}] // \frac{r_0 + Z_L}{1 + g_{m1} r_0} \quad (1)$$

Where, $R_P = \frac{L_S^2 \omega^2}{R_S} + R_S$.

Where r_0 is the channel resistance of M_1. While C_{gs1} resonates with L_S, the input impedance can then be approximated as:

$$Z_{\text{in}} = jwL_1 + R_P // \frac{1}{j\omega C_{gs}} // \frac{r_0 + Z_L}{1 + g_{m1} r_0} \quad (2)$$



a The Proposed IMN Topology *b The equivalent small signal model of the circuit in Fig. 2a*

Figure 1: CG LNA topology

It can be observed that R_p adds an additional degree of freedom to the input match design, and alleviates the restricted g_{m1} value for input matching. Eq. (2) illustrate that gm1 is not restricted to 20 mS if resistance R_s is adjusted to maintain the desired 50 Ω input matching. Note that there will be a small DC voltage drop across R_s that will consume headroom at the output, but the increased flexibility in the input matching design justifies the trade-off.

2.2 Noise analysis and noise cancelling technique

We can characterize the performance of a particular receiver element by its NF, which is the ratio of actual output noise of the element to that which would remain if the element itself did not introduce noise. The total NF of a receiver system (a chain of stages) can be calculated using the Friss formula as follows:

$$NF = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1 G_2} + \ldots + \frac{(NF_n - 1)}{G_1 G_2 \cdots G_{n-1}} \quad (3)$$

The total system NF equals the sum of the NF of the first stage (NF_1) plus that of the second stage (NF_2) minus 1 divided by the total gain of the previous stage (G_1) and so on. This result suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases, implying that the first

few stages in a cascade are the most critical. It is understandable that the total NF is dominated by the NF_1, which is the NF of the LNA.

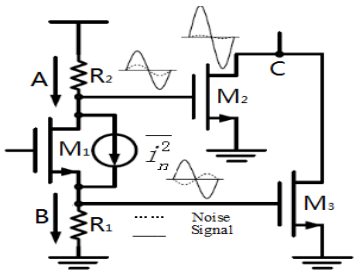


Figure 2: Principle of noise cancelling technique

Noise canceling technique is an effective technique to reduce the NF to a lower level. Fig. 3 shows the small-signal schematic of the presented LNA. The purpose of noise cancelling is to decouple the input matching with the NF by cancelling the output noise from the matching device. In the presented LNA, a common-gate amplifier with a source feedback resistance is used as the input stage to get a good input impedance matching. The main noise source of the LNA is the input matching NMOS transistor M_1. The noise current $\overline{i_n^2}$ of M1 flows into R1 but out from R2, which makes the noise voltages from M1 at node A and B in the opposite phases while the signals are in phases. These noise voltages are converted to currents and added together at node C. With the noise cancelling technique, the noise current of M1 flowing to the output So the noise effect to the output from M1 will be reduced and what's more this noise will be completely cancelled at some special values of R1, R2, g_{m2}, g_{m3}. By properly designing g_{m2} and gm3, the noise contributed by M1 can be cancelled at the output.

2.3 Proposed UWB LNA circuit

The CG stage failed to provide enough gain at higher frequency which is the main unacceptable outcome for UWB applications. Thus, the design of the CG amplifier adopts a multilevel structure to improve the circuit performance. Fig. 3 shows the complete schematic diagram of the 3.1–10.6 GHz CMOS UWB LNA, in which the important device parameters are labelled.

We propose a UWB CG LNA architecture in Fig. 3. The first stage of the UWB LNA configuration consists of the CG input stage (M_1) and gm-boosted amplifier (M_6) for input wideband matching, the CG stage with low input impedance characteristic and broadband behavior, provides NF that is almost independent of the frequency of operation. The CG stage also eliminates the Miller effect and hence provides better isolation from the output return signal. Then the CS second stage (M_2) for gain improvement followed by an output buffer (M_4, M_5) used to drive 50 Ω. which adopted a new T-match IMN composed of a series L_S-R_S, interconnection-line inductance L_1, active gm-boosted technology and C_{gs}-g_{m1} of transistor M1 to enhance the matching bandwidth of the IMN LNA. An inverting common-source amplifier M_6 is introduced between the gate and source of M_1 to boost its effective transconductance G_m from gm1 to $(1+g_{m6}R_{B1})g_{m1}$, which can improve the input match, reduce NF and increase the S_{21}. The self-body bias and current reused technique are used to reduce power consumption further. In order to compensate for the power gain, a CS amplifier using gain peaking techniques is adopted in the second stage. C_G is the coupling capacitor, and C_b is the bypass capacitor. The proposed amplifier is the current reuse CG-CS LNA with capacitive inter-stage coupling except the extra inductor L_G, which value is adjusted for the series resonance with the input capacitance of M_2 to provide a low impedance path. In order to cancelling the noise of CG transistor, we utilizing noise cancelling technique to cancel the noise of the first stage. The values of L_D and C_b affect gain flatness in the design employing the stagger tuning technique. The peaking inductor L_D and the parasitic capacitances at the drain terminal of M_1 and the source terminal of M_2 were parallel resonant at the lower corner frequency (3.2GHz), while the peaking inductor L_C and C_{gs5} were series resonant at the upper corner frequency (10.4 GHz). In this way, flat power gain, high power gain, flat and low noise factor were achieved.

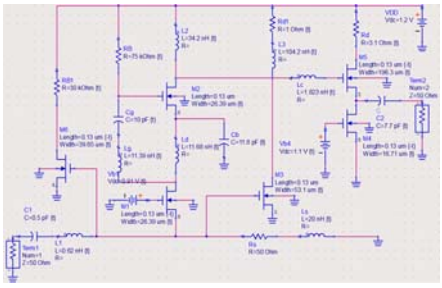


Figure 3: Schematic of the proposed LNA

3. Simulation results and discussions

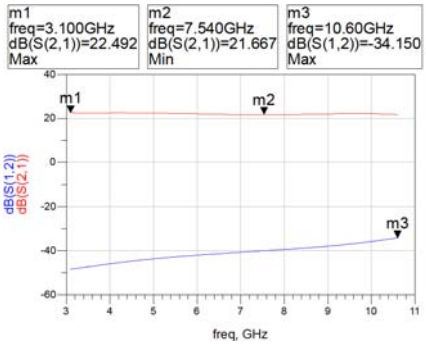


Figure 4: Simulated S_{21} and S_{12} against frequency characteristics of 3.1-10.6 GHz UWB LNA

The designed circuit of Fig. 4 is simulated with Agilent Advanced Design System (ADS) tools in TSMC 0.13 µm RF CMOS technology. Results of S-parameters, noise and stable are shown in Fig. 4 – Fig. 6. The simulated S21 and S12 characteristics are shown in Fig. 4. The simulated S21 shows and average power gain of 22.0795 dB with the bandwidth from 3.1 to 10.6 GHz, which is relatively high for wideband amplifiers. The full band gain ripple is about ± 0.4125 dB. The simulated S12 is less than -34.15 dB in the frequency range of 3.1-10.6 GHz, which indicating the proposed UWB LNA can have a good stability performance. S_{12} is below -34.15 dB due to RF chock inductor (L_D) and bypass capacitor (C_b) between transistor M_1 and M_2 within the required bandwidth. The better reverse S_{12} can reduce the latter local oscillation leakage arising from the capacitive paths and the substrate coupling. The value of input return loss (S_{11}) and output return loss (S_{22}) is shown in Fig. 5, the value of S_{11} is below -15.635 dB. S_{22} is less than -16.903 dB. As shown in Fig. 6, the simulated result clearly shows an excellent NF of 2.232-2.696 dB in the frequency range of 3.1-10.6 GHz. The minimum NF is 2.232 dB at 10.6 GHz and the maximum NF is 2.696 dB at 5.36 GHz, with an average NF of 2.464 dB.

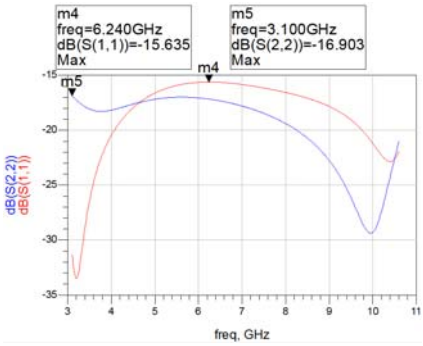


Figure 5: Simulated S_{11} and S_{22} against frequency characteristics of 3.1-10.6 GHz UWB LNA

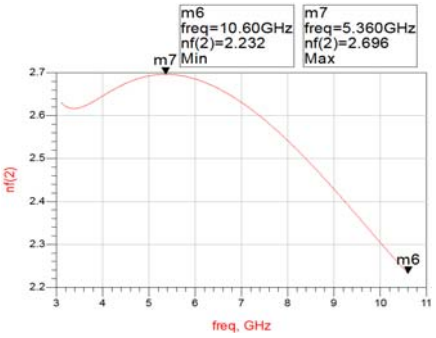


Figure 6: Simulated NF against frequency characteristics of 3.1-10.6 GHz UWB LNA

A comparison of our proposed LNA with other recently published LNAs is presented in Table 1. The FOM is also included in the table and defined in Eq. (4), which was confirmed (Muhammed and Rezaul Hasan (2013)).

$$FOM = \frac{|S_{21}| * BW}{(|NF| - 1) * P_D} \quad (4)$$

Where $|S_{21}|$ indicates the average power/voltage gain, BW indicate the bandwidth in GHz, $|NF|$ represents the average noise figure and P_D represents the power dissipation in milliwatts (mW). The proposed architecture achieves considerably high FOM compared to most of the recently published popular designs.

Table 1: Comparison of the simulated results of the proposed LNA with other recently published.

	This work	Ahmed and Carlos(2011)	Jing et al (2014)	Habid et al (2013)	Shim el al (2013)	Habid et al (2015)	Wan et al (2015)
Technology(μm)	0.13	0.13	0.18	0.13	0.18	0.13	0.18
BW(GHz)	3.1-10.6	3.1-10.6	3.1-10.6	3.1-10.6	3.1-10.6	3.1-10.6	3.1-10.6
S21(dB)	22.0795±0.4125	16*	20.65*	19.5±1.5	11.3*	10.24#	14.4*
NF (dB)	2.464±0.0.232	3.9*	2.79*	2.45±1.45	4.15*	2.5*	2.6*
P_D(mW)	3.996	10	33	4.1	8.2	17.92	9.0
FOM(GHz/mW)	28.31	4.14	2.62	24.6	3.28	2.86	7.5

* Average value
\# Maximum value

3. Conclusion

A high S_{21} and low NF 3.1-10.6 GHz CG CMOS UWB LNA using active g_m-boosted technology, T-match input network, self-body-bias, current reused and noise cancelling technique has been developed in TSMC 0.13 μm RF CMOS technology. The feasibility of the proposed UWB LNA for achieving high and flat power gain, good reverse isolation, good input and output matching, and excellent noise performance in this paper. It has a high and relatively flat S_{21} performance across the entire 7500 MHz bandwidth. The simulated result shows that the proposed UWB LNA has high and flat S_{21} of 21.667 to 22.492 dB, good S_{11} < -15.635 dB, S_{12} <-34.15 dB, S_{22} < -16.903 dB, and low and flat NF of 2.232 to 2.696 dB over the 3.1-10.6GHz band of interest. At the supply voltage of 1.2 V, the amplifier stage draw the current of 3.33 mA resulting in a power consumption of 3.996 mW, the output buffer stage draws the current of 7.07 mA resulting in a power consumption of 8.484 mW. The results of the proposed UWB LNA indicate that is very suitable for 3.1-10.6GHz UWB system applications.

Acknowledgments

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